

What is claimed:

1 1. A semiconductor device having a non-volatile memory transistor,
2 comprising:
3 a semiconductor layer;
4 a floating gate disposed over the semiconductor layer through a first dielectric layer
5 as a gate dielectric layer;
6 a second dielectric layer that contacts at least a part of the floating gate and is
7 capable of functioning as a tunneling dielectric layer;
8 a control gate formed over the second dielectric layer; and
9 an impurity diffusion layer that forms a source region or a drain region formed in the
10 semiconductor layer,
11 wherein a conduction layer is provided above the floating gate, and the conduction
12 layer entirely overlaps the floating gate.

1 2. A semiconductor device having a non-volatile memory transistor according
2 to claim 1, wherein the conduction layer outwardly protrudes from an end of the floating
3 gate as viewed in a plan view, and a width of a portion of the conduction layer that
4 outwardly protrudes from the end of the floating gate as viewed in a plan view is 0.5 μm or
5 smaller.

1 3. A semiconductor device having a non-volatile memory transistor according
2 to claim 1, wherein a side end of the conduction layer formed above the floating gate and an
3 end of the floating gate are aligned with each other.

1 4. A semiconductor device having a non-volatile memory transistor according
2 to claim 1, wherein a width of the conduction layer above a region other than a region where
3 the floating gate is formed is narrower than a width of the conduction layer above the region
4 where the floating gate is formed.

1 5. A semiconductor device having a non-volatile memory transistor according
2 to claim 1, wherein the conduction layer is electrically connected to the semiconductor layer.

1 6. A semiconductor having a non-volatile memory transistor device,
2 comprising:
3 a semiconductor layer;
4 a floating gate disposed over the semiconductor layer through a first dielectric layer
5 as a gate dielectric layer;
6 a second dielectric layer that contacts at least a part of the floating gate and is
7 capable of functioning as a tunneling dielectric layer;
8 a control gate formed over the second dielectric layer; and
9 an impurity diffusion layer that forms a source region or a drain region formed in the
10 semiconductor layer,
11 wherein a plurality of conduction layers are formed at different levels above the
12 floating gate, and the floating gate is entirely overlapped by the plurality of conduction
13 layers as viewed in a plan view.

1 7. A semiconductor device having a non-volatile memory transistor according
2 to claim 6, wherein at least one of the conduction layers outwardly protrudes from an end of
3 the floating gate as viewed in a plan view, and a width of a portion of the conduction layer
4 that outwardly protrudes from the end of the floating gate as viewed in a plan view is 0.5 μm
5 or smaller.

1 8. A semiconductor device having a non-volatile memory transistor according
2 to claim 6, wherein a side end of the at least one of the conduction layers and an end of the
3 floating gate are aligned with each other.

1 9. A semiconductor device having a non-volatile memory transistor according
2 to claim 6, wherein the conduction layer is electrically connected to the semiconductor layer.

1 10. A semiconductor device having a non-volatile memory transistor, comprising
2 a non-volatile memory transistor including a semiconductor layer, a floating gate disposed
3 above the semiconductor layer, and a control gate formed above the floating gate, wherein a
4 conduction layer is provided vertically above the floating gate at least in a region where the
5 control gate is not disposed vertically above the floating gate.

1 11. A semiconductor device having a non-volatile memory transistor, comprising
2 a non-volatile memory transistor including a semiconductor layer, a floating gate disposed
3 above the semiconductor layer, and a control gate formed above the floating gate,
4 wherein a conduction layer is provided above the non-volatile memory transistor and
5 a portion of the conduction layer is located vertically above the floating gate, and
6 a width of the conduction layer located vertically above the floating gate is formed to
7 be greater than a width of the floating gate.

1 12. A semiconductor device having a non-volatile memory transistor according
2 to claim 11, wherein a width of the conduction layer located other than vertically above the
3 floating gate is formed to be smaller than a width of the conduction layer located vertically
4 above the floating gate.

1 13. A semiconductor device having a non-volatile memory transistor according
2 to claim 12, wherein the conduction layer is a wiring layer.

1 14. A semiconductor device having a non-volatile memory transistor according
2 to claim 13, wherein the wiring layer is a lowermost wiring layer.

1 15. A semiconductor device having a non-volatile memory transistor, comprising
2 a non-volatile memory transistor including a semiconductor layer, a floating gate disposed
3 above the semiconductor layer, and a control gate disposed above the floating gate,
4 wherein a plurality of conduction layers having a multiple layered structure are
5 provided above the non-volatile memory transistor, and
6 at least one conduction layer among the plurality of conduction layers is provided
7 vertically above the floating gate at least in a region where the control gate is not disposed
8 vertically above the floating gate.

1 16. A semiconductor device having a non-volatile memory transistor according
2 to claim 15, where the conduction layers are wiring layers.

1 17. A semiconductor device having a non-volatile memory transistor according
2 to claim 15, further comprising:
3 a first dielectric layer that defines a gate dielectric layer disposed between the
4 semiconductor layer and the floating gate;
5 a second dielectric layer that contacts at least a part of the floating gate and is
6 capable of functioning as a tunneling dielectric layer; and
7 an impurity diffusion layer that forms a source region or a drain region formed in the
8 semiconductor layer.

1 18. A semiconductor device having a non-volatile memory transistor according
2 to claim 1, wherein the non-volatile memory transistor comprises a first circuit region, and
3 wherein the semiconductor device further comprises a second circuit region mix-mounted
4 therein.

1 19. A semiconductor device having a non-volatile memory transistor according
2 to claim 18, wherein the second circuit region includes at least a logic circuit.

1 20. A semiconductor device having a non-volatile memory transistor according
2 to claim 10, further comprising:
3 a first dielectric layer that defines a gate dielectric layer disposed between the
4 semiconductor layer and the floating gate;
5 a second dielectric layer that contacts at least a part of the floating gate and is
6 capable of functioning as a tunneling dielectric layer; and
7 an impurity diffusion layer that forms a source region or a drain region formed in the
8 semiconductor layer,

1 21. A semiconductor device having a non-volatile memory transistor according
2 to claim 15, wherein the non-volatile memory transistor comprises a first circuit region, and
3 wherein the semiconductor device further comprises a second circuit region mix-mounted
4 therein.

1 22. A semiconductor device having a non-volatile memory transistor according
2 to claim 21, wherein the second circuit region includes at least a logic circuit.

1 23. A semiconductor device having a non-volatile memory transistor, comprising
2 a semiconductor layer;
3 a floating gate disposed over the semiconductor layer through a first dielectric layer
4 comprising a gate dielectric layer;
5 a second dielectric layer that contacts at least a part of the floating gate and is
6 capable of functioning as a tunneling dielectric layer;
7 a control gate formed over the second dielectric layer; and
8 one or more conduction layers formed over the floating gate, the floating gate
9 including an upper surface, wherein a line normal to any portion of the upper surface will
10 contact at least one of the one or more conduction layers over the floating gate.

1 24. A method for manufacturing a semiconductor device having a non-volatile
2 memory transistor, comprising:
3 forming a first dielectric layer comprising a gate dielectric layer on a substrate;
4 forming a floating gate over the gate dielectric layer;
5 forming a second dielectric layer that contacts at least a part of the floating gate and
6 is capable of functioning as a tunneling dielectric layer;
7 forming a control gate over the second dielectric layer;
8 forming an impurity diffusion layer that forms a source region or a drain region in
9 the semiconductor layer; and
10 forming a conduction layer above the floating gate so that a portion of the
11 conduction layer is positioned vertically above the floating gate, where the portion of the
12 conduction layer overlaps the entire floating gate.

1 25. A method for manufacturing a semiconductor device having a non-volatile
2 memory transistor, comprising:
3 forming a floating gate above a semiconductor layer;
4 forming a control gate above the floating gate; and
5 forming a conduction layer vertically above the floating gate at least in a region
6 where the control gate is not disposed vertically above the floating gate.

1 26. A method as in claim 25, comprising forming the conduction layer to have a
2 width greater than that of the floating gate in a region where the conduction layer is disposed
3 vertically above the floating gate.

- 1 27. A method for manufacturing a semiconductor device having a non-volatile
2 memory transistor, comprising:
3 forming a floating gate above a semiconductor layer;
4 forming a control gate above the floating gate,
5 forming a plurality of conduction layers having a multiple layered structure above
6 the non-volatile memory transistor, and
7 wherein at least one of the conduction layers is formed vertically above the floating
8 gate at least in a region where the control gate is not disposed vertically above the floating
9 gate.

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